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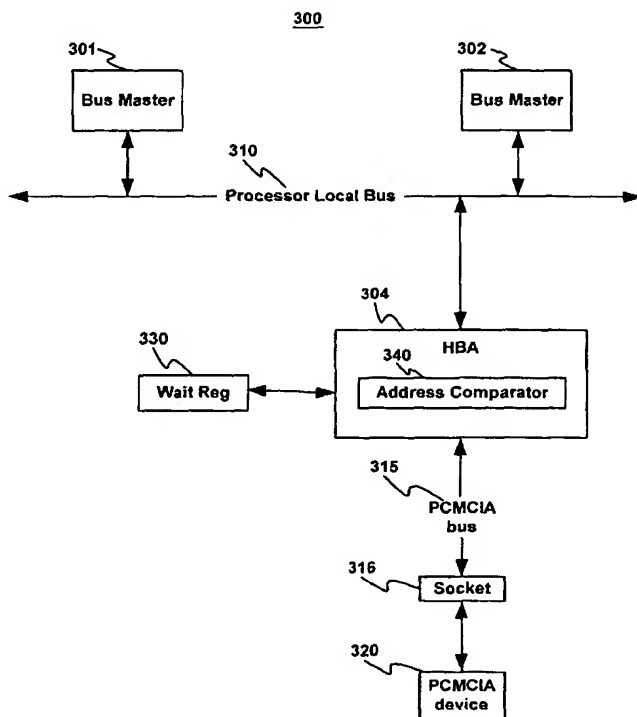
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- (51) International Patent Classification⁷: **G06F 13/42**, 13/364, 13/40 (72) Inventor: **MEIYAPPAN, Subramanian, S.**; 505 West Baseline Road, #1140, Tempe, AZ 85283 (US).
- (21) International Application Number: **PCT/US01/02710** (74) Agents: **GALLENSON, Mavis, S. et al.**; Ladas & Parry, 5670 Wilshire Boulevard, Suite 2100, Los Angeles, CA 90036-5679 (US).
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- (71) Applicant (*for MC only*): **PHILIPS SEMICONDUCTORS, INC.** [US/US]; 811 East Arques Avenue, Sunnyvale, CA 94088 (US). (88) Date of publication of the international search report: 16 January 2003
- (71) Applicant (*for all designated States except MC*): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoulevard 1, NL-5621 BA Eindhoven (NL). For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: DATA TRANSACTION ACCESS SYSTEM AND METHOD



(57) Abstract: A data transaction access system for an embedded microprocessor coupled to a PCMCIA bus device. A bus master and a host bus adapter are coupled to a local bus for enabling communication between the bus master and a PCMCIA device. The PCMCIA device is coupled to the host bus adapter via a PCMCIA bus. The bus master uses the local bus to communicate with the PCMCIA device via the host bus adapter. A wait register is coupled to the host bus adapter to receive a delay input from the PCMCIA device describing a latency period of the device when completing a data transaction. Where the latency period described by the delay input is less than a predetermined amount, the host bus adapter is configured to insert wait states into the data transaction of the bus master. When the latency period is greater than the predetermined amount, the host bus adapter is configured to retry the data transaction of the bus master. Alternatively, the wait register is adapted to couple the delay input to the bus master such that the bus master initiates a subsequent access to the PCMCIA device at the expiration of the latency period in order to efficiently complete the subsequent access to the target PCI agent. Alternatively, the wait register is coupled to an arbiter such that the arbiter does not grant the local bus to the bus master for a subsequent access until the expiration of the latency period.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06F13/42 G06F13/364 G06F13/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

WPI Data, IBM-TDB, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 872 799 A (NEC CORPORATION) 21 October 1998 (1998-10-21) the whole document	1
Y	US 5 715 410 A (KIM) 3 February 1998 (1998-02-03) column 1, line 45 -column 3, line 18 figures 1,2	1
A	WO 96 38773 A (NATIONAL SEMICONDUCTOR CORPORATION) 5 December 1996 (1996-12-05) page 2, line 20 -page 4, line 33 figures 1,2	1-16

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Information on patent family members

Intel onal Application No

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